CLAIMS:

What is claimed is:

1. A dynamic circuit, said dynamic circuit comprising:

a logic portion adapted for processing logic of said dynamic domino circuit;

a first dynamic output portion coupled to said logic portion, said first dynamic output portion having a first dynamic node for dynamically holding a first data;

a second dynamic output portion coupled to said logic portion, said second dynamic output portion having a second dynamic node for dynamically holding a second data;

a third dynamic output portion coupled to said logic portion, said third dynamic output portion having a third dynamic node for dynamically holding a third data;

a first and a second transistors having their gates coupled to said first dynamic node, said first transistor having its drain coupled to said second dynamic node, said second transistor having its drain coupled to said third dynamic node;

a third and a fourth transistors having their gates coupled to said second dynamic node, said third transistor having its drain coupled to said first dynamic node, said fourth transistor having its drain coupled to said third dynamic node; and

a fifth and a sixth transistors having their gates coupled to said third dynamic node, said fifth transistor having its drain coupled to said first dynamic node, said sixth transistor having its drain coupled to said second dynamic node.

2. A dynamic adder, said dynamic adder comprising:

a plurality of dynamic circuits arranged into a plurality of levels, wherein each of said plurality of dynamic circuit implements a three term carry logic, wherein inversion of any of said three terms at a dynamic circuit is implemented as a function of true terms.

3. A multiplexer, said multiplexer comprising:

a latch built into said multiplexer; and

a first and a second dynamic select inputs to said multiplexer, wherein said multiplexer functions as a latch using said latch when said first and said second dynamic select inputs are precharged to logic zero, and wherein said multiplexer functions as a multiplexer when said first and said second select inputs are evaluated to their respective logic values.